

Pi 2 Design

**PI2AES 2.0 2.0
Digital Pro Audio Hat
Hardware Reference Manual
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Table of Contents

1 Warranty.....	3
2 Operating Specifications.....	4
2.1 PI2AES 2.0 Operating specifications	4
3 Overview	5
3.1 Introduction	5
3.2 Block Diagram.....	5
4 On-Board Devices	7
4.1 Overview.....	7
4.1 PI2AES 2.0 I2C Bus Devices.....	7
4.1 WM8804 SPDIF Transmitter.....	7
4.1.1 WM8804 SPDIF Transmitter Notes	8
4.2 Dual High Resolution NDK Clocks.....	8
4.3 RS-422 Differential Transmitter	8
4.4 I2S Parallel Buffer	8
4.5 I2S Differential Driver	8
4.6 Audio Data Rate and Power LED's.....	8
5 RPi GPIO.....	9
5.1 Overview.....	9
5.1.1 RPi GPIO Notes.....	10
6 PI2AES 2.0 Power.....	11
6.1 Overview.....	11
7 PI2AES 2.0 Software	12
7.1 Overview.....	12
8 Top Side Connectors	13
8.1 Overview.....	13
8.2 J1 – DC Jack.....	16
8.3 P1 – 40-Pin GPIO Header	16
8.1 P3 – XLR Balanced Output.....	16
8.2 P4 – I2S Over HDMI.....	16
8.3 U9 – Combo RCA/Opto Transmitter	17
8.4 D1 – Status LEDs.....	17
9 Document Revisions.....	18
10 Errata.....	19
10.1 Overview	19

List of Tables

Table 1 – PI2AES 2.0 Operating Specifications	4
Table 2 – PI2AES 2.0 I2C Bus Devices	7
Table 3 – RPi to WM8804 Connections	8
Table 4 – CPU GPIO Pin Assignments	10
Table 5 – I2S Over HDMI Pinout.....	17
Table 6 – Document Revisions	18

List of Figures

Figure 1 – PI2AES 2.0 Block Diagram	6
Figure 2 – PI2AES 2.0 Power, Simplified Block Diagram	11
Figure 3 – PI2AES 2.0 Top View	15
Figure 4 – PI2AES 2.0 Front View (shown mounted on Raspberry Pi 4)	15
Figure 5 – PI2AES 2.0 Side View (shown mounted on Raspberry Pi 4)	16

I WARRANTY

The enclosed product ("the Product"), a part of the P2 2 Design Shield/Hat series, is warranted by Pi 2 Design for a period of one year for reasonable development, testing and use, all as further described and defined below. This warranty runs solely to the individual or entity purchasing the Product and is not transferable or assignable in any respect. This warranty is valid only for so long as the product is used intact as shipped from Pi 2 Design. Any attempt or effort to alter the Product, including but not limited to any attempt to solder, de-solder, unplug, replace, add or affix any part or component of or onto the Product, other than components specifically intended for the user to plug and unplug into appropriate sockets and/or Connectors to facilitate user programming, development and deployment, all as specifically described and authorized in this Product Hardware Reference Manual, shall void this warranty in all respects. Coverage under this warranty requires that the Product be used and stored at all times in conditions with proper electrostatic protection necessary and appropriate for a complex electronic device. These conditions include proper temperature, humidity, radiation, atmosphere and voltage (standard commercial environment, 0C to +70C, <60%RH). Any Product that has been modified without the express, prior written consent of Pi 2 Design is not covered by this warranty. The use or connection of any test or bus Connector, adapter or component with any device other than a Pi 2 Design Connector or adapter shall void this warranty and the warranty of all other components, parts and modules connected to the rest of the system. Pi 2 Design shall not be responsible for any damage to the Product as a result of a customer's use or application of circuitry not developed or approved by Pi 2 Design for use on or in connection with the Product.

This warranty does not cover defects caused by electrical or temperature fluctuations or from stress resulting from or caused by abuse, misuse or misapplication of the Product. Any evidence of tampering with the serial number on the Product shall immediately void this warranty. This Product is not intended to be used on or embedded in or otherwise used in connection with any life-sustaining or life-saving product and this warranty is not applicable nor is Pi 2 Design liable in any respect if the Product is so used. Notwithstanding anything to the contrary herein, Pi 2 Design expressly disclaims any implied warranty of merchantability or implied warranty of fitness for a particular purpose in connection with the manufacture or use of the Product.

2 OPERATING SPECIFICATIONS

2.1 PI2AES 2.0 OPERATING SPECIFICATIONS

The PI2AES 2.0 conforms to the following specifications:

Specification	Value
Dimensions	85mm x 56.5mm
Weight	~10g
Storage Temperature	-20C to +85C
Operating Temperature	0C to +70C
Humidity	0% to 95% RH, Non-Condensing
Input Voltage (VIN)	+5V, +/-5%
Power Consumption	250mw Typical, 1W Maximum

Table 1 – PI2AES 2.0 Operating Specifications

3 OVERVIEW

3.1 INTRODUCTION

The PI2AES 2.0, designed and manufactured by PI 2 Design, is a professional I/O Shield designed to bring Professional Studio Grade Audio to the Raspberry Pi® family of Single Board Computers. This low-cost Shield converts the Raspberry Pi® I2S Interface to High Definition Digital Audio Coax, OPTO and Balanced XLR.

The addition of I2S LVDS Differential over HDMI allows the PI2AES 2.0 to interface with virtually any High Performance DAC on the market.

The major features of the PI2AES 2.0 are as follows:

- **FORM FACTOR** – Raspberry Pi® Shield Size w/40-Pin mating connector.
- **AES TRANSMITTER** – The industry standard WM8804 converts the RPi I2S stream to AES3/SPDIF formatted data at 24-Bit up to 192Khz Frame Rate
- **COAX OUTPUT** – A 1:1 Isolation Transformer provides Bit Perfect Impedance Controlled Coaxial Transmission of the Digital Audio Data
- **SPDIF OPTICAL OUTPUT** – Isolated Optical Transmitter Drives Consumer Level DAC and AVR
- **BALANCED OUTPUT** – An RS-422 Transmitter coupled with a 1:1 Isolation Transformer allows the transmission of balanced audio data via the Professional Audio Standard XLR Connector
- **DIFFERENTIAL I2S OUTPUT** – A DS2063 Differential Transmitters is used to drive the I2S Bus over a standard HDMI Connector. The Pinout is Selectable Between the PS Audio and Gustard Standards.
- **HIGH RESOLUTION CLOCKS** – A pair of Ultra-Low Noise NDK NZ2520SDA oscillators allow the WM8804 to operate in non-PLL mode for the lowest possible noise.
- **ULTRA-LOW NOISE LDO's** – Ultra-Low Noise LT3045 LDO (0.9uV noise and 80dB PSRR) is used to power the WM8804 AES Transmitter, while a 2nd LT3045 LDO powers the NDK Clocks.
- **LOW NOISE PCB LAYOUT** – Constructed with 4-layer Split Ground PCB with noise reduction techniques refined from years of High-Speed Mixed-Signal Design work

3.2 BLOCK DIAGRAM

Refer to the following figure for a block diagram of the PI2AES 2.0 Shield.

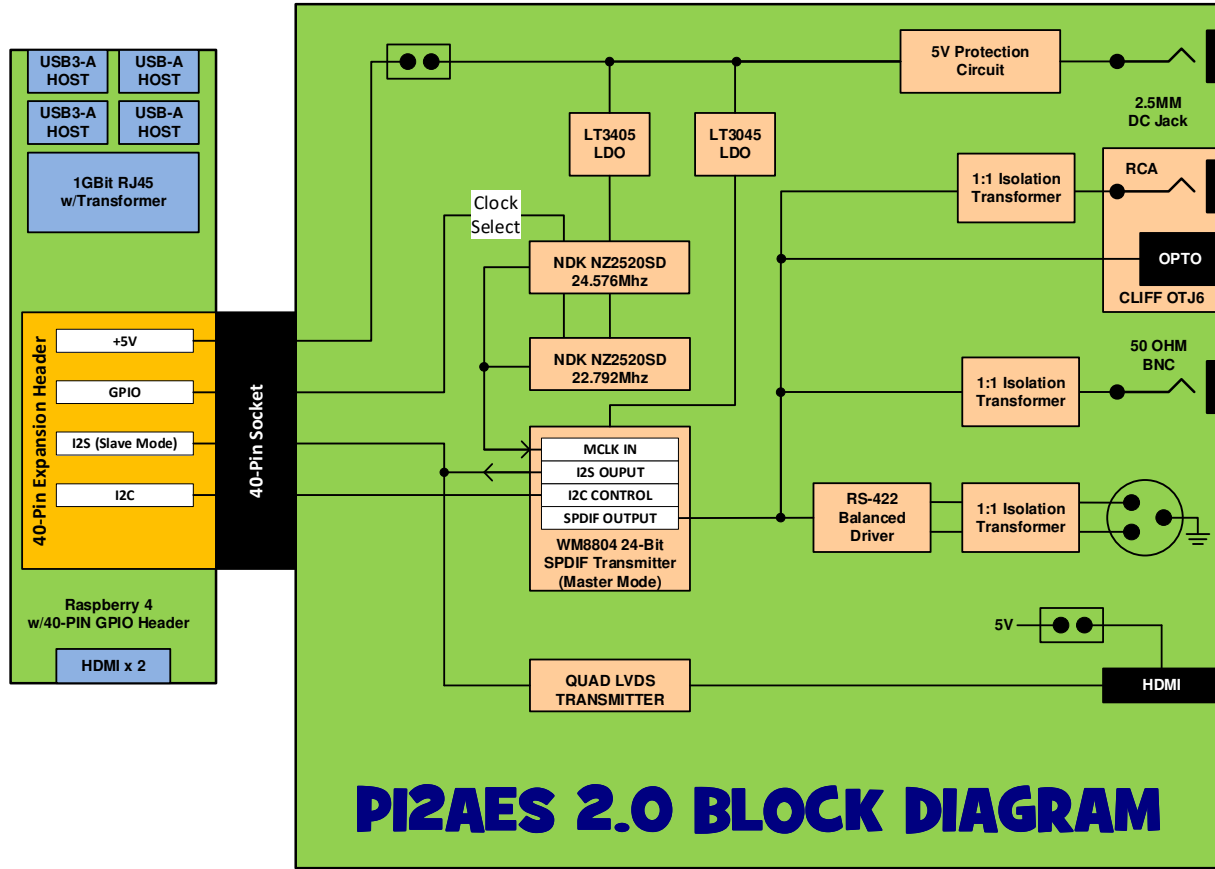


Figure 1 – PI2AES 2.0 Block Diagram

4 ON-BOARD DEVICES

4.1 OVERVIEW

The PI2AES 2.0 interfaces to the RPi via the 40-Pin GPIO Connector. This section describes in detail the devices located on the PI2AES 2.0.

4.1 PI2AES 2.0 I2C BUS DEVICES

The following table describes the CPU I2C Bus usage of the PI2AES 2.0. Most of these addresses are set by the startup script supplied by Pi2Design. Refer to the respective device documentation for more detail.

I2C Bus	7-Bit I2C Address	Description
I2C	0x3B	WM8804 SPDIF Transmitter

Table 2 – PI2AES 2.0 I2C Bus Devices

4.1 WM8804 SPDIF TRANSMITTER

At the core of the PI2AES 2.0 is the Cirrus Logic WM8804 AES Digital Audio Transmitter. This device interfaces to the Raspberry Pi via I2S and I2C. The signals used to interface with the WM8804 are shown in the following table.

WM8804 Signal	RPi Signal	Description
MCLK	-	Unused
BCLK	BCLK	I2S Bit Clock Output to Pi
LRCLK	LRCLK	I2S Word Clock Output to Pi
SDIN	SDOUT	I2S Serial Audio Data Input from Pi
SCL	SCL	I2C Clock from Pi
SDA	SDA	I2C Data to/from Pi
XIN	GPIO5	1 = Select 22.5792Mhz Input Clock for 44.1Khz, 88.2Khz and 176.4Khz Frame Rates
XIN	GPIO6	1 = Select 24.576Mhz Input Clock for 48Khz, 96Khz and 192Khz Frame Rates

TXO	-	AES3/SPDIF encoded digital audio output
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Table 3 – RPi to WM8804 Connections

4.1.1 WM8804 SPDIF TRANSMITTER NOTES

1. The WM8804 is controlled using the I2C port. Refer to the WM8804 documentation and Pi 2 Design supplied driver code for more detail.
2. The PI2AES 2.0 is designed to operate the WM8804 in Master mode. In this mode the WM8804 receives its master clock from XIN and drives MCLK (unused), BCLK and LRCLK to the Pi. Serial Data in is received from Pi.
3. Pi GPIO's 6 and 13 are used to select the desired clock input. GPIO 6 and 13 are pulled low by default. CAUTION - Do not select more than one clock at a time!

4.2 DUAL HIGH RESOLUTION NDK CLOCKS

A pair of NDK NZ2520SDA Ultra-Low Noise clocks provide the critical timing signals for the WM8804. They are selected via Raspberry PI GPIO5 (22.5792Mhz) and GPIO6 (24.576Mhz).

4.3 RS-422 DIFFERENTIAL TRANSMITTER

An RS-422 Differential Transmitter accepts the SPDIF output from the WM8804 and sends it as a balanced pair to the 1:1 Isolation Transformer and then to the XLR connector.

4.4 I2S PARALLEL BUFFER

A 74FCT125 CMOS Buffer is used to drive the I2S signals (MCLK, BCKL, LRCLK and SDO) to the I2S Expansion Header. This device is designed to drive the I2S Bus short distances (<12 inches).

4.5 I2S DIFFERENTIAL DRIVER

A DS2063 Quad Differential LVDS Driver takes the I2S Bus and converts each signal into a balanced differential signal. This is then connected to the HDMI connector. This device is designed to drive the I2S Bus up to 3 meters.

4.6 AUDIO DATA RATE AND POWER LED'S

Three LEDs are used to provide visual indication of: Power On (Green), Audio Data Rate of 48/96/192Khz (Yellow) and Audio Data Rate of 44.1/88.2/176.4Khz (Red).

5 RPI GPIO

5.1 OVERVIEW

The PI2AES 2.0 uses a number of signals from the RPi GPIO header for control and status purposes. This usage is defined in the following table.

RPI PIN	DIR	AF	PUP/PDN	PI2AES 2.0 Name	Description/Notes
1	-	-	-	-	RPi +3.3V - Unused
2	-	-	-	+5V	+5V Power to/from the RPi
3	I/O	Y	PUP	I2C_SDA	I2C Bus Data
4	-	-	-	+5V	+5V Power to/from the RPi
5	OUT	Y	PUP	I2C_SCL	I2C Bus Clock
6	-	-	-	GND	
7	OUT	-	-	GPIO4	Unused
8	-	-	-	GPIO14	Unused
9	-	-	-	GND	Unused
10	-	-	-	GPIO15	Unused
11	-	-	-	GPIO17	Unused
12	IN	Y	-	BCLK	I2S Bit Clock from WM8804
13	-	-	-	GPIO27	Unused
14	-	-	-	GND	
15	-	-	-	GPIO22	Unused
16	-	-	-	GPIO23	Unused
17	-	-	-	-	RPi +3.3V - Unused
18	-	-	-	GPIO24	Unused
19	-	-	-	GPIO10	Unused
20	-	-	-	GND	
21	-	-	-	GPIO9	Unused

RPi PIN	DIR	AF	PUP/PDN	PI2AES 2.0 Name	Description/Notes
22	-	-	-	GPIO25	Unused
23	-	-	-	GPIO11	Unused
24	-	-	-	GPIO8	Unused
25	-	-	-	GND	
26	-	-	-	GPIO1	Unused
27	I/O	Y	-	ID_SDA	Unused
28	OUT	Y	-	ID_SCL	Unused
29	-	-	PDN	GPIO5	1 = Select 22.5792Mhz Clock Input to WM8804
30	-	-	-	GND	
31	OUT	-	PDN	GPIO6	1 = Select 24.576Mhz Clock Input to WM8804
32	-	-	-	GPIO12	Unused
33	OUT	-	-	GPIO13	Unused
34	-	-	-	GND	
35	IN	Y	-	LRCLK	I2S Left/Right Clock from WM8804
36	-	-	-	GPIO16	Unused
37	-	-	-	GPIO26	Unused
38	-	-	-	GPIO20	Unused
39	-	-	-	GND	
40	OUT	Y	-	SDOUT	Pi I2S Serial Audio Data Out

Table 4 – CPU GPIO Pin Assignments

5.1.1 RPI GPIO NOTES

1. DIR is from the point of view of the RPi.
2. Y in the Alternate Function (AF) column indicates that the use of this pin requires the pin to be assigned to the function as defined by the RPi specifications.
3. PUP/PDN indicates if the GPIO should have its associated Pullup (PUP) or Pulldown (PDN) resistor enabled.
4. An asterisk “*” at the beginning of the name indicates a low true signal.

6 PI2AES 2.0 POWER

6.1 OVERVIEW

The PI2AES 2.0 is designed to be powered from either the Raspberry PI GPIO Pins 1 and 3, or from an external +5V (+/-10%) source. Jumper W2, when installed, allows the PI2AES 2.0 to be powered from the Raspberry PI. When jumper W2 is removed, separate 5V power must be supplied to the PI2AES 2.0 and the Raspberry PI.

Note, the on-board protection circuit ensures proper operation when jumper W2 is removed and power is applied via J1 and from the Pi (P1) simultaneously.

See the below block diagram for a simplified view of the PI2AES 2.0 power.

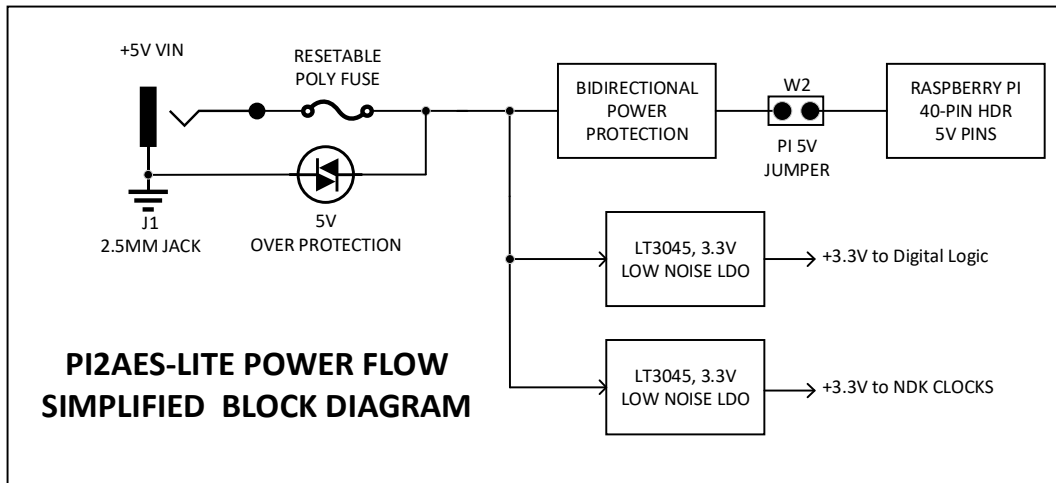


Figure 2 – PI2AES 2.0 Power, Simplified Block Diagram

7 PI2AES 2.0 SOFTWARE

7.1 OVERVIEW

Due to the various resources interfaced on the PI2AES 2.0, both internal and external to the RPi, it is necessary to initialize a large number of CPU registers and external devices before correct operation can begin. These values and their proper sequencing are beyond the scope of this document. For most Raspberry Pi Software, the HifiBerry Digi+ Pro driver should be used.

8 TOP SIDE CONNECTORS

8.1 OVERVIEW

This section provides the type, location, and pinout for the various connectors on the PI2AES 2.0. Top View and Front View are shown in the following 3D renders.

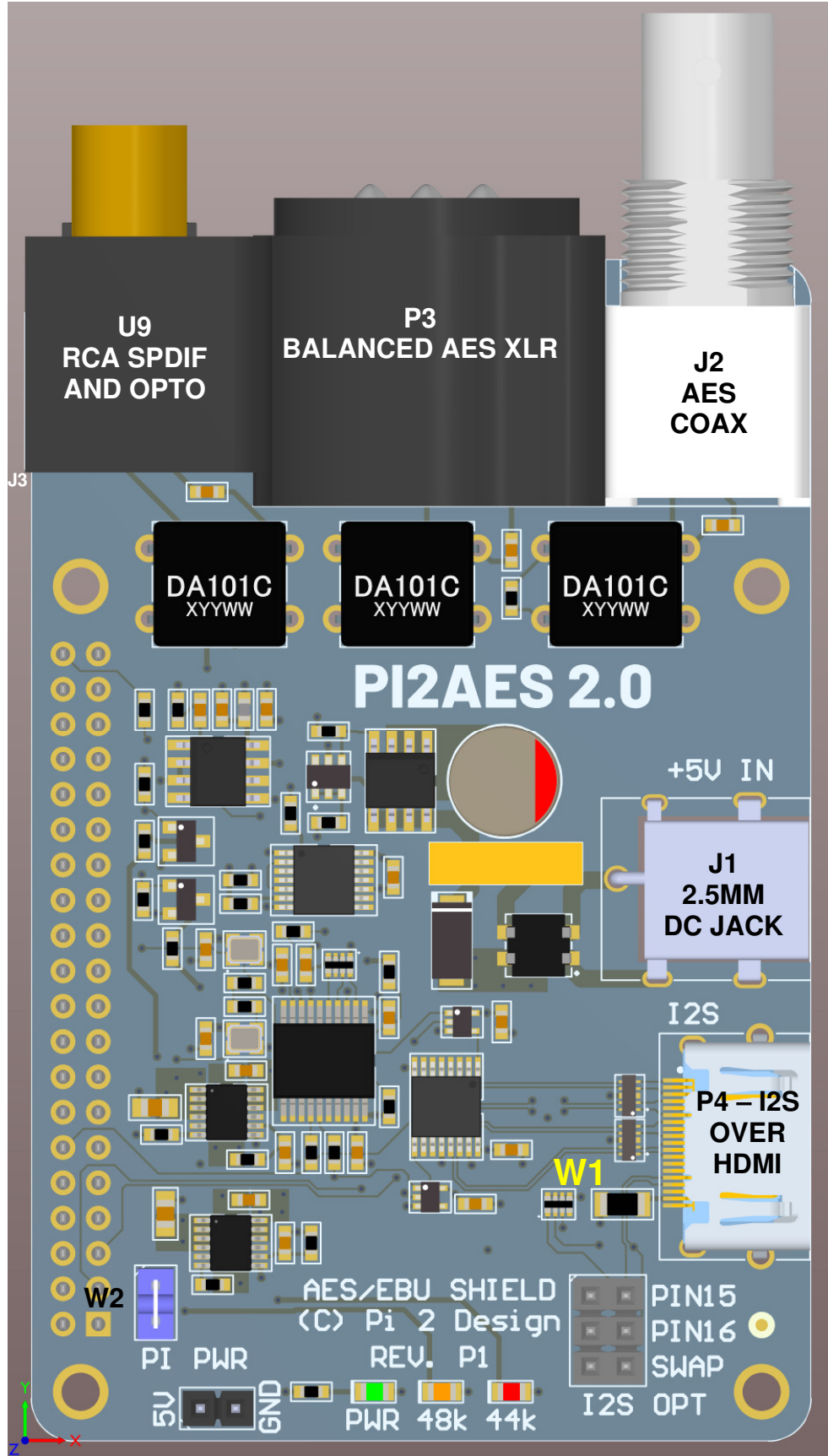


Figure 3 – PI2AES 2.0 Top View

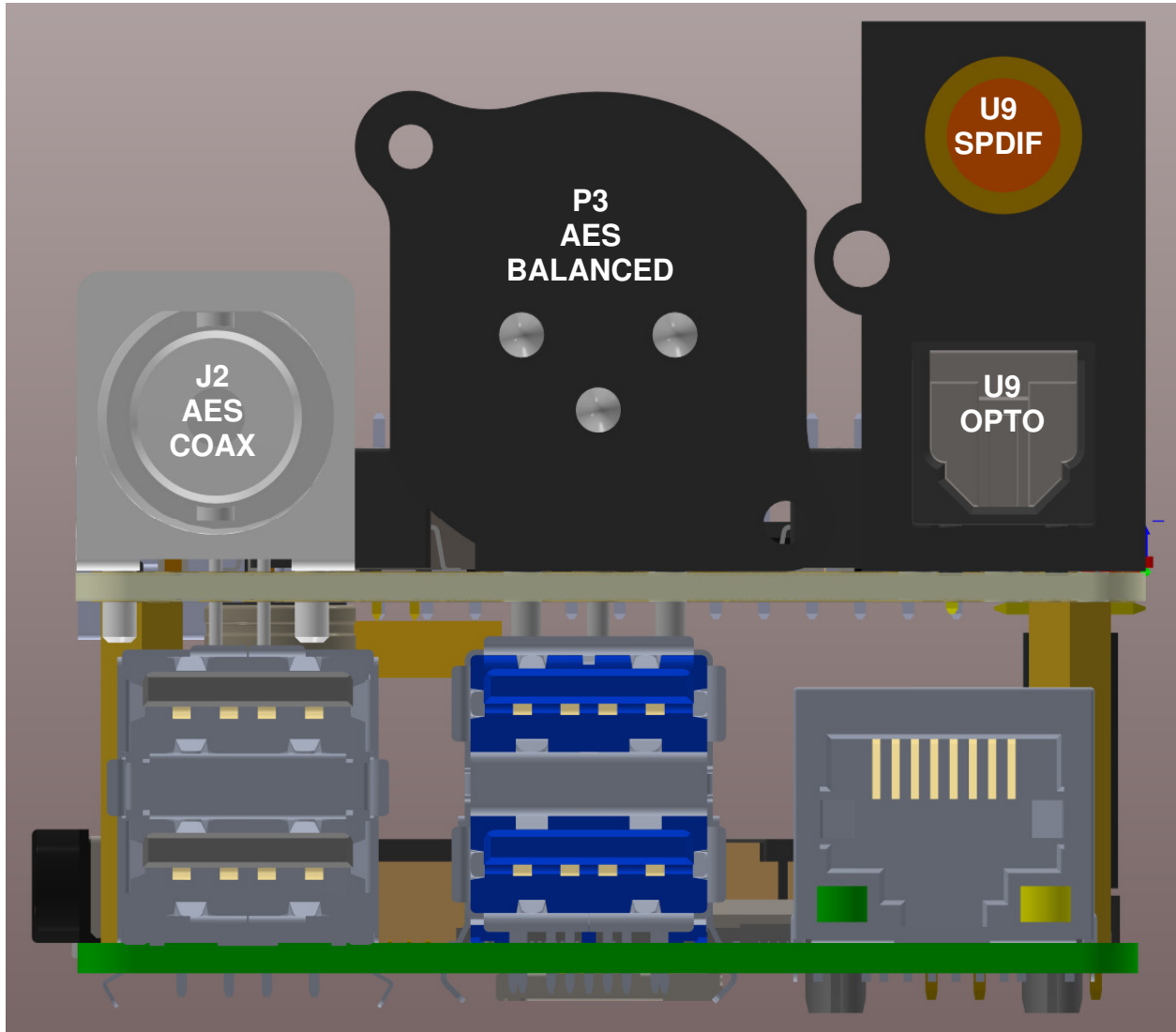


Figure 4 – PI2AES 2.0 Front View (shown mounted on Raspberry Pi 4)



Figure 5 – PI2AES 2.0 Side View (shown mounted on Raspberry Pi 4)

8.2 J1 – DC JACK

This jack is designed to accept a 5.5mm x 2.5mm center positive plug for external power in. Voltage must be +5V +/-5% or damage may occur. DO NOT USE THE +24V SUPPLY from the original PI2AES.

8.3 P1 – 40-PIN GPIO HEADER

This is a standard 40-Pin .1” Dual Row Female Header. It is designed to accept a Raspberry Pi single board and conforms to the standard Raspberry Pi 40-Pin GPIO Header pinout.

8.1 P3 – XLR BALANCED OUTPUT

P3 is a 3-Pin XLR Connector. This 100-ohm connector carries the balanced digital audio output.

8.2 P4 – I2S OVER HDMI

P4 is a standard HDMI Connector that carries the Differential I2S signal. Pinout conforms to either the PS Audio (default) or Gustard standards. The Pinout for P4 is shown in the following table. **%FIXME%**

P4 PIN	Name	W1 Jumper 5-6 In PS Audio Pinout	W1 Jumper 5-6 Out Gustard Pinout
1	TD2+	SDO- Data Minus	SDO+ Data Plus
2	GND	Ground	Ground
3	TD2-	SDO+ Data Plus	SDO- Data Minus
4	TD1+	BCK+ Bit Clock Plus	BCK+ Bit Clock Plus
5	GND	Ground	Ground
6	TD1-	BCK- Bit Clock Minus	BCK- Bit Clock Minus
7	TD0+	WCK- Word Clock Minus	WCK+ Word Clock Plus
8	GND	Ground	Ground
9	TDO-	WCK+ Word Clock Plus	WCK- Word Clock Minus
10	TDC+	MCK+ Master Clock Plus	MCK+ Master Clock Plus
11	GND	Ground	Ground
12	TDC -	MCK- Master Clock Minus	MCK- Master Clock Minus
13	NC	No Connect	No Connect
14	NC	No Connect	No Connect
15	PIN15	W1 Jumper 1-2 In – High	W1 Jumper 1-2 Out - Low
16	PIN16	W1 Jumper 3-4 In – High	W1 Jumper 3-4 Out - Low
17	GND	Ground	Ground
18	+5V	DDC Power – 100ma MAX	
19	NC	No Connect	No Connect

Table 5 – I2S Over HDMI Pinout

8.3 U9 – COMBO RCA/OPTO TRANSMITTER

U9 is a Cliff OTJ6 that contains the RCA for AES COAX digital audio output and a Toslink Transmitter for SPDIF Optical digital audio output.

8.4 DI – STATUS LEDS

There are multiple LEDs on the PI2AES 2.0: Power ON (Green, P3.x only); 48Khz/96Khz/192Khz Clock (Yellow); and 44.1Khz/88.2Khz/176.4Khz Clock (Red).

9 DOCUMENT REVISIONS

Date	Revision	Change
04/19/2023	P1.0	First Release
07/12/2023	P1.1	Updated Section 6 to include note regarding voltage drop
02/04/2024	P1.2	Re-worded Section 6 to define power options

Table 6 – Document Revisions

IO ERRATA

10.1 OVERVIEW

There are currently no known errata for the PI2AES 2.0 Rev. P1.